

## DESCRIPTION

FREQUENCY DIVIDING CIRCUIT AND MULTIMODE RADIO USING THE SAME

### 5 TECHNICAL FIELD

[0001]

This invention relates to a frequency dividing circuit made up of frequency dividers and a multimode radio that can use a plurality of radio systems by using the frequency dividing  
10 circuit to switch frequencies.

### BACKGROUND ART

[0002]

A multimode radio in a related art is described in patent  
15 document 1. FIG. 14 shows a configuration example of the multimode radio in the related art compatible with radio system A and radio system B described in patent document 1.

[0003]

In FIG. 14, an antenna 901 is shared between the radio  
20 system A and the radio system B. The antenna 901 is connected to a duplexer 902 of the radio system A and a duplexer 903 of the radio system B. In a transmission system, an in-phase baseband transmission signal is input from an in-phase baseband input terminal 916 to a low-pass filter 914. The in-phase  
25 baseband transmission signal is modulated by a quadrature

modulator 913 and becomes an in-phase intermediate frequency transmission signal. A quadrature baseband transmission signal is input from a quadrature baseband input terminal 917 to a low-pass filter 915. The quadrature baseband transmission signal is modulated by the quadrature modulator 913 and becomes a quadrature intermediate frequency transmission signal. The in-phase intermediate frequency transmission signal and the quadrature intermediate frequency transmission signal are amplified by a variable gain amplifier 912 and unnecessary frequency components are removed through a low-pass filter 911. The in-phase intermediate frequency transmission signal and the quadrature intermediate frequency transmission signal are up converted by a transmission mixer 910 and are subjected to gain control by a variable gain amplifier 909 and becomes a transmission signal of the radio system A or the radio system B. When the multimode radio operates with the radio system A, a high frequency switch 908 connects to a power amplifier 906. When the multimode radio operates with the radio system B, the high frequency switch 908 connects to a power amplifier 907. The transmission signal of the radio system A is transmitted from the antenna 901 through an isolator 904 and the duplexer 902, and the transmission signal of the radio system B is transmitted from the antenna 901 through an isolator 905 and the duplexer 903.

[0004]

In a reception system, when the multimode radio operates with the radio system A, a reception signal of the radio system A received at the antenna 901 is amplified by a low noise amplifier 919 through the duplexer 902. The amplified reception signal is subjected to frequency conversion by a reception mixer 921 and then passes through an intermediate frequency filter 923 corresponding to the reception frequency and becomes an intermediate frequency reception signal. The intermediate frequency reception signal is input to a variable gain amplifier 926 through an intermediate frequency switch 925. When the multimode radio operates with the radio system B, a reception signal of the radio system B received at the antenna 901 is amplified by a low noise amplifier 920 through the duplexer 903. The amplified reception signal is subjected to frequency conversion by a reception mixer 922 and then passes through an intermediate frequency filter 924 corresponding to the reception frequency and becomes an intermediate frequency reception signal. The intermediate frequency reception signal is input to the variable gain amplifier 926 through the intermediate frequency switch 925. The amplified intermediate frequency reception signal is demodulated by a quadrature demodulator 927 and becomes an in-phase baseband reception signal and a quadrature baseband reception signal. The in-phase baseband reception signal passes through a low-pass filter 928 and is output from an in-phase baseband

output terminal 930. The quadrature baseband reception signal passes through a low-pass filter 929 and is output from a quadrature baseband output terminal 931.

[0005]

5           A first local oscillator 918 outputs a transmission local oscillation signal corresponding to the radio system A and the radio system B to a transmission mixer 910. The first local oscillator 918 outputs a reception local oscillation signal corresponding to the radio system A and the radio system B to  
10   reception mixers 921 and 922. A second local oscillator 933 outputs a modulation local oscillation signal to the quadrature modulator 913 through a frequency dividing section 936. The second local oscillator 933 outputs a demodulation local oscillation signal to the quadrature demodulator 927.

15   [0006]

          The frequency dividing section 936 is made up of frequency dividers and switches setting the frequency dividing counts corresponding to the modulation local oscillation signal and the demodulation local oscillation signal of the  
20   radio system A and the modulation local oscillation signal and the demodulation local oscillation signal of the radio system B. A frequency divider 951 corresponds to the modulation local oscillation signal of the radio system A. A frequency divider 952 corresponds to the modulation local oscillation signal of  
25   the radio system B. The frequency divider 951 and the frequency

divider 952 are switched by a switch 955. A frequency divider 953 corresponds to the demodulation local oscillation signal of the radio system A. A frequency divider 954 corresponds to the demodulation local oscillation signal of the radio system B. The frequency divider 953 and the frequency divider 954 are switched by a switch 956. At the radio system A operation time, the switch 955 connects to the frequency divider 951 and the switch 956 connects to the frequency divider 953. At the radio system B operation time, the switch 955 connects to the frequency divider 952 and the switch 956 connects to the frequency divider 954. The multimode radio includes as many frequency dividers as the number of covered radio systems and the number of modulation and demodulation combinations. As the frequency dividers are switched by the switch, the multimode radio in the related art can switch among radio systems using different frequency bands without increasing the number of local oscillators.

[0007]

As an example of sharing and combining frequency dividers, a first frequency divider for dividing output of a local oscillator and a second frequency divider for dividing output of the first frequency divider are included. It is assumed that the output of the first frequency divider corresponds to a first radio system and the output of the second frequency divider corresponds to a second radio system. The frequency

divider inputs an in-phase local oscillation signal and a quadrature local oscillation signal having a 90° phase difference to a quadrature modulator and a quadrature demodulator. To obtain output of the first frequency divider, the second frequency divider is connected to either of in-phase local oscillation signal output and quadrature local oscillation signal output of the first frequency divider. Here, it is assumed that the in-phase local oscillation signal output of the first frequency divider connects to the second frequency divider. When the multimode radio operates with the first radio system, the second frequency divider need not be operated and may be turned off by a switch. However, it is difficult to implement an open/short switch in IC in an actual circuit and the circuit operation is turned on/off by current control (non-patent document 1).

Patent document 1: JP-A-9-261106 (p.4-p.5, FIG. 2)

Non-patent document 1: "Analog IC no kinou kairo sekkei nyuumon" written by AOKI Hidehiko, CQ Shuppansha, p.168

## DISCLOSURE OF THE INVENTION

### PROBLEMS THAT THE INVENTION IS TO SOLVE

[0008]

However, in the configuration in the related art shown above in (patent document 1), as many frequency dividers as the number of radio systems covered by the multimode radio are

required. Further, the frequency divider having a positive frequency dividing count is provided by using 2-frequency-dividing circuits and 3-frequency-dividing circuits in combination and therefore has a problem of increasing the circuit scale. It is an object of the invention to lessen the circuit scale by sharing and combining frequency dividers in setting the frequency dividing count about frequency dividers of the configuration in the related art. [0009]

Incidentally, in the configuration in the related art shown above in (patent document 1), the first frequency divider for dividing output of the local oscillator and the second frequency divider for dividing output of the first frequency divider are included and the circuit operation is turned on/off by current control as shown in (non-patent document 1). The off circuit is connected to the path which is on as a load and affects the path which is on. When the output of the first frequency divider is input to the quadrature modulator or the quadrature demodulator, the second frequency divider which is off is affected. Therefore, an error occurs in the  $90^\circ$  phase difference between the in-phase local oscillation signal and the quadrature local oscillation signal of the first frequency divider. The in-phase local oscillation signal and the quadrature local oscillation signal input to the quadrature modulator and the quadrature demodulator need keep the  $90^\circ$  phase

difference therebetween with high accuracy. However, if the frequency dividers are shared and combined, the impedance symmetry of the first frequency divider output terminal worsens because of the circuit which is off, and a phases error occurs;  
5 this is a problem. The invention is intended for solving the above-described problems in the related arts and it is an object of the invention to provide a multimode radio whose circuit scale is lessened and simplified by sharing frequency dividers and eliminating the output phase error.

10

#### MEANS FOR SOLVING THE PROBLEMS

[0010]

To solve the problems in the related arts, the first frequency dividing circuit of the invention is a frequency  
15 dividing circuit including a first frequency divider for dividing output of a local oscillator and outputting a first in-phase local oscillation signal and a first quadrature local oscillation signal, a second frequency divider being connected to the first in-phase local oscillation signal output for  
20 dividing the first in-phase local oscillation signal and outputting a second in-phase local oscillation signal and a second quadrature local oscillation signal, and phase correction means for keeping the phase difference between the first in-phase local oscillation signal and the first  
25 quadrature local oscillation signal at 90 degrees. It is made



possible to share and combine the frequency dividers and the circuit scale can be kept small and be simplified.

[0011]

The second frequency dividing circuit of the invention  
5 is a frequency dividing circuit including a first frequency divider for dividing output of a local oscillator and outputting a first in-phase local oscillation signal and a first quadrature local oscillation signal, a second frequency divider being connected to the first quadrature local  
10 oscillation signal output for dividing the first quadrature local oscillation signal and outputting a second in-phase local oscillation signal and a second quadrature local oscillation signal, and phase correction means for keeping the phase difference between the first in-phase local oscillation signal  
15 and the first quadrature local oscillation signal at 90 degrees. It is made possible to share and combine the frequency dividers and the circuit scale can be kept small and be simplified.

[0012]

The third frequency dividing circuit of the invention  
20 is a frequency dividing circuit wherein in the first frequency dividing circuit of the invention, the phase correction means includes a dummy circuit being connected to the first quadrature local oscillation signal output and having input impedance equal to that of the second frequency divider. It  
25 is made possible to share and combine the frequency dividers,

the circuit scale can be lessened and simplified, and the dummy circuit having the input impedance equal to that of the second frequency divider is included, whereby the phase difference between the first in-phase local oscillation signal and the first quadrature local oscillation signal can be kept at high accuracy.

[0013]

The fourth frequency dividing circuit of the invention is a frequency dividing circuit wherein in the second frequency dividing circuit of the invention, the phase correction means includes a dummy circuit being connected to the first in-phase local oscillation signal output and having input impedance equal to that of the second frequency divider. It is made possible to share and combine the frequency dividers, the circuit scale can be lessened and simplified, and the dummy circuit having the input impedance equal to that of the second frequency divider is included, whereby the phase difference between the first in-phase local oscillation signal and the first quadrature local oscillation signal can be kept at high accuracy.

[0014]

The fifth frequency dividing circuit of the invention is a frequency dividing circuit wherein in the first or second frequency dividing circuit of the invention, the phase correction means includes a control section for controlling

the current of an in-phase output amplifier of the first frequency divider and a quadrature output amplifier of the first frequency divider. It is made possible to share and combine the frequency dividers, the circuit scale can be lessened and simplified, and the current of the in-phase output amplifier and the quadrature output amplifier is controlled, so that the phase difference between the first in-phase local oscillation signal and the first quadrature local oscillation signal can be kept at high accuracy.

10 [0015]

The sixth frequency dividing circuit of the invention is a frequency divider circuit wherein in the first frequency dividing circuit of the invention, the phase correction means includes a control section for controlling the current of a dummy circuit connected to the first quadrature local oscillation signal output, an in-phase output amplifier of the first frequency divider, and a quadrature output amplifier of the first frequency divider. It is made possible to share and combine the frequency dividers, the circuit scale can be lessened and simplified, the dummy circuit having the input impedance equal to that of the second frequency divider is included, and the current of the in-phase output amplifier and the quadrature output amplifier is controlled, so that the phase difference between the first in-phase local oscillation signal and the first quadrature local oscillation signal can

be kept at high accuracy.

[0016]

The seventh frequency dividing circuit of the invention is a frequency divider circuit wherein in the second frequency  
5 dividing circuit of the invention, the phase correction means includes a control section for controlling the current of a dummy circuit connected to the first in-phase local oscillation signal output, an in-phase output amplifier of the first frequency divider, and a quadrature output amplifier of the  
10 first frequency divider. It is made possible to share and combine the frequency dividers, the circuit scale can be lessened and simplified, the dummy circuit having the input impedance equal to that of the second frequency divider is included, and the current of the in-phase output amplifier and  
15 the quadrature output amplifier is controlled, so that the phase difference between the first in-phase local oscillation signal and the first quadrature local oscillation signal can be kept at high accuracy.

[0017]

20 The dummy circuit may be a circuit including a resistor and a capacitor, may be an amplifier having the same circuit configuration as an input amplifier of the second frequency divider, or may have the same circuit configuration as a part of an input amplifier of the second frequency divider.

25 [0018]

When the dummy circuit has the same circuit configuration as the input amplifier of the second frequency divider, the control section may control the current of the dummy circuit and the input amplifier.

5 [0019]

The first multimode radio of the invention is a multimode radio including any of the frequency dividing circuits described above, and includes a local oscillator for outputting a local oscillation signal to the first frequency divider, a first quadrature modulator to which the first in-phase local oscillation signal and the first quadrature local oscillation signal are input, the first quadrature modulator for performing quadrature modulation of an in-phase baseband transmission signal and a quadrature baseband transmission signal and outputting a first transmission signal having a first frequency, and a second quadrature modulator to which the second in-phase local oscillation signal and the second quadrature local oscillation signal are input, the second quadrature modulator for performing quadrature modulation of the in-phase baseband transmission signal and the quadrature baseband transmission signal and outputting a second transmission signal having a second frequency. It is made possible to share and combine the frequency dividers in the transmission system, and the circuit scale can be lessened and simplified.

25 [0020]

The multimode radio may further include a control section being connected to the second frequency divider, the first quadrature modulator, and the second quadrature modulator for switching a mode between a mode of transmitting the first transmission signal and a mode of transmitting the second transmission signal.

[0021]

The second multimode radio of the invention is a multimode radio including any of the frequency dividing circuits described above, and includes a local oscillator for outputting a local oscillation signal to the first frequency divider, a first quadrature demodulator to which the first in-phase local oscillation signal and the first quadrature local oscillation signal are input, the first quadrature demodulator for performing quadrature demodulation of a first reception signal having a first frequency and outputting an in-phase baseband reception signal and a quadrature baseband reception signal, and a second quadrature demodulator to which the second in-phase local oscillation signal and the second quadrature local oscillation signal are input, the second quadrature demodulator for performing quadrature demodulation of a second reception signal having a second frequency and outputting the in-phase baseband reception signal and the quadrature baseband reception signal. It is made possible to share and combine the frequency dividers in the reception

system, and the circuit scale can be lessened and simplified.

[0022]

The multimode radio may further include a control section being connected to the second frequency divider, the first  
5 quadrature demodulator, and the second quadrature demodulator for switching a mode between a mode of receiving the first reception signal and a mode of receiving the second reception signal.

[0023]

10 The third multimode radio of the invention is a multimode radio including any of the frequency dividing circuits described above, and includes a local oscillator for outputting a local oscillation signal to the first frequency divider, a first quadrature modulator to which the first in-phase local  
15 oscillation signal and the first quadrature local oscillation signal are input, the first quadrature modulator for performing quadrature modulation of an in-phase baseband transmission signal and a quadrature baseband transmission signal and outputting a first transmission signal having a first frequency,  
20 a second quadrature modulator to which the second in-phase local oscillation signal and the second quadrature local oscillation signal are input, the second quadrature modulator for performing quadrature modulation of the in-phase baseband transmission signal and the quadrature baseband transmission  
25 signal and outputting a second transmission signal having a

second frequency, a first quadrature demodulator to which the first in-phase local oscillation signal and the first quadrature local oscillation signal are input, the first quadrature demodulator for performing quadrature demodulation  
5 of a first reception signal having the first frequency and outputting an in-phase baseband reception signal and a quadrature baseband reception signal, and a second quadrature demodulator to which the second in-phase local oscillation signal and the second quadrature local oscillation signal are  
10 input, the second quadrature demodulator for performing quadrature demodulation of a second reception signal having the second frequency and outputting the in-phase baseband reception signal and the quadrature baseband reception signal.  
It is made possible to share and combine the frequency dividers  
15 in the transmission-reception system, and the circuit scale can be lessened and simplified.

[0024]

The multimode radio may further include a control section being connected to the second frequency divider, the including  
20 a control section being connected to the second frequency divider, the first quadrature modulator, the second quadrature modulator, the first quadrature demodulator, and the second quadrature demodulator for switching a mode between a mode of transmitting the first transmission signal and receiving the  
25 first reception signal and a mode of transmitting the second



transmission signal and receiving the second reception signal.

#### ADVANTAGES OF THE INVENTION

[0025]

5           A multimode radio whose circuit scale is lessened and simplified can be provided according to the multimode radio of the invention.

#### BRIEF DESCRIPTION OF THE DRAWINGS

10   [0026]

[FIG. 1]    A diagram to show the configuration of a multimode radio in a first embodiment of the invention.

[FIG. 2]    A circuit diagram to show a current control method in the first embodiment of the invention.

15   [FIG. 3]   A diagram to show the configuration of a frequency dividing section of the multimode radio in the first embodiment of the invention.

[FIG. 4]    A diagram to show the configuration of a multimode radio in a second embodiment of the invention.

20   [FIG. 5]   A diagram to show the configuration of a frequency dividing section of the multimode radio in the second embodiment of the invention.

[FIG. 6]    diagram to show the configuration of a multimode radio in a third embodiment of the invention.

25   [FIG. 7]   A diagram to show the configuration of a frequency

dividing section of the multimode radio in the third embodiment of the invention.

[FIG. 8] A diagram to show the circuit configuration of an input amplifier of a frequency divider 601 in the third  
5 embodiment of the invention.

[FIG. 9] A diagram to show the configuration of a multimode radio in a fourth embodiment of the invention.

[FIG. 10] A diagram to show the configuration of a frequency dividing section of the multimode radio in the fourth  
10 embodiment of the invention.

[FIG. 11] A diagram to show the circuit configuration of an in-phase output amplifier of a frequency divider 701 in the fourth embodiment of the invention.

[FIG. 12] A diagram to show the configuration of a multimode  
15 radio in a fifth embodiment of the invention.

[FIG. 13] A diagram to show the configuration of a frequency divider of the multimode radio in the fifth embodiment of the invention.

[FIG. 14] A diagram to show the configuration of a multimode  
20 radio in a related art.

#### DESCRIPTION OF REFERENCE NUMERALS

[0027]

1 Antenna

25 2 Duplexer

|    |    |                                     |
|----|----|-------------------------------------|
|    | 3  | Duplexer                            |
|    | 4  | Power amplifier                     |
|    | 5  | Power amplifier                     |
|    | 6  | Quadrature modulator                |
| 5  | 7  | Quadrature modulator                |
|    | 8  | In-phase baseband input terminal    |
|    | 9  | Quadrature baseband input terminal  |
|    | 10 | Low noise amplifier                 |
|    | 11 | Low noise amplifier                 |
| 10 | 12 | Quadrature demodulator              |
|    | 13 | Quadrature demodulator              |
|    | 14 | Low-pass filter                     |
|    | 15 | Low-pass filter                     |
|    | 16 | In-phase baseband output terminal   |
| 15 | 17 | Quadrature baseband output terminal |
|    | 18 | Local oscillator                    |
|    | 19 | Frequency divider                   |
|    | 20 | Frequency divider                   |
|    | 21 | Dummy circuit                       |
| 20 | 22 | Frequency dividing section          |
|    | 23 | Control section                     |
|    | 31 | Low noise amplifier                 |
|    | 32 | Low noise amplifier                 |
|    | 33 | Reception mixer                     |
| 25 | 34 | Reception mixer                     |

35 Quadrature demodulator  
 36 Quadrature demodulator  
 37 Dummy circuit  
 38 Frequency divider  
 5 39 Dummy circuit  
 40 Frequency divider  
 100 Multimode radio  
 201 Transistor  
 202 Transistor  
 10 203 Resistor  
 204 Resistor  
 205 Transistor  
 206 Current control terminal  
 301 Input amplifier  
 15 302 Flip-flop circuit  
 303 Flip-flop circuit  
 304 In-phase output amplifier  
 305 Quadrature output amplifier  
 306 Input amplifier  
 20 307 Flip-flop circuit  
 308 Flip-flop circuit  
 309 In-phase output amplifier  
 310 Quadrature output amplifier  
 400 Multimode radio  
 25 501 Input amplifier

502 Flip-flop circuit  
 503 Flip-flop circuit  
 504 In-phase output amplifier  
 505 Quadrature output amplifier  
 5 506 Amplifier  
 600 Multimode radio  
 601 Frequency divider  
 602 Dummy circuit  
 603 Frequency divider  
 10 604 Input amplification circuit  
 605 Transistor  
 606 Transistor  
 607 Load resistor  
 608 Load resistor  
 15 609 Transistor  
 610 Resistor  
 700 Multimode radio  
 701 Frequency divider  
 702 Frequency dividing section  
 20 703 In-phase output amplifier  
 704 Quadrature output amplifier  
 705 Transistor  
 706 Transistor  
 707 Load resistor  
 25 708 Load resistor

|    |     |                                    |
|----|-----|------------------------------------|
|    | 709 | Transistor                         |
|    | 710 | Resistor                           |
|    | 800 | Multimode radio                    |
|    | 801 | Frequency dividing section         |
| 5  | 901 | Antenna                            |
|    | 902 | Duplexer                           |
|    | 903 | Duplexer                           |
|    | 904 | Isolator                           |
|    | 905 | Isolator                           |
| 10 | 906 | Power amplifier                    |
|    | 907 | Power amplifier                    |
|    | 908 | High frequency switch              |
|    | 909 | Variable gain amplifier            |
|    | 910 | Transmission mixer                 |
| 15 | 911 | Low-pass filter                    |
|    | 912 | Variable gain amplifier            |
|    | 913 | Quadrature modulator               |
|    | 914 | Low-pass filter                    |
|    | 915 | Low-pass filter                    |
| 20 | 916 | In-phase baseband input terminal   |
|    | 917 | Quadrature baseband input terminal |
|    | 918 | First local oscillator             |
|    | 919 | Low noise amplifier                |
|    | 920 | Low noise amplifier                |
| 25 | 921 | Reception mixer                    |

922 Reception mixer  
923 Intermediate frequency filter  
924 Intermediate frequency filter  
925 Intermediate frequency filter  
5 926 Variable gain amplifier  
927 Quadrature demodulator  
928 Low-pass filter  
929 Low-pass filter  
930 In-phase baseband output terminal  
10 931 Quadrature baseband output terminal  
933 Second local oscillator  
934 Frequency dividing section  
936 Frequency divider  
951 Frequency divider  
15 952 Frequency divider  
953 Frequency divider  
954 Frequency divider  
955 Switch  
956 Switch

20

BEST MODE FOR CARRYING OUT THE INVENTION

[0028]

Embodiments of the invention will be discussed with the  
accompanying drawings.

25 [0029]

(First embodiment)

In a first embodiment, the operation of a multimode radio for covering two frequency bands will be discussed.

[0030]

5           FIG. 1 shows a configuration example of a multimode radio in the first embodiment. A multimode radio 100 in the first embodiment uses a first frequency band and a second frequency band. In the description to follow, as a specific example, a radio system is GSM, the first frequency band is 1800-MHz  
10 band, and the second frequency band is 900-MHz band, but any other radio system and frequency band may be adopted. The operation modes are 1800-MHz mode and 900-MHz mode.

[0031]

          In FIG. 1, an antenna 1 is shared between the 1800-MHz  
15 band and the 900-MHz band. The antenna 1 is connected to a duplexer 2 corresponding to the 1800-MHz band and a duplexer 3 corresponding to the 900-MHz band. First, a transmission system will be discussed. An in-phase baseband input terminal 8 and a quadrature baseband input terminal 9 are connected to  
20 a quadrature modulator 6 corresponding to the 1800-MHz band and a quadrature modulator 7 corresponding to the 900-MHz band. When the multimode radio 100 operates in the 1800-MHz mode, a baseband transmission signal is input from the in-phase baseband input terminal 8 and the quadrature baseband input  
25 terminal 9.       The baseband transmission signal is



quadrature-modulated by the quadrature modulator 6 and becomes  
a 1800-MHz band transmission signal. The transmission signal  
is amplified by a power amplifier 4 corresponding to the  
1800-MHz band. The amplified transmission signal is  
5 transmitted from the antenna 1 through the duplexer 2.

[0032]

When the multimode radio 100 operates in the 900-MHz mode,  
likewise a baseband transmission signal is input from the  
in-phase baseband input terminal 8 and the quadrature baseband  
10 input terminal 9. The baseband transmission signal is  
quadrature-modulated by the quadrature modulator 7 and becomes  
a 900-MHz band transmission signal. The transmission signal  
is amplified by a power amplifier 5 corresponding to the 900-MHz  
band. The amplified transmission signal is transmitted from  
15 the antenna 1 through the duplexer 3.

[0033]

Next, a reception system will be discussed. When the  
multimode radio 100 operates in the 1800-MHz mode, a reception  
signal received at the antenna 1 is input to a low noise  
20 amplifier 10 corresponding to the 1800-MHz band through the  
duplexer 2. The reception signal is amplified by the low noise  
amplifier 10. The amplified reception signal is  
quadrature-demodulated by a quadrature demodulator 12  
corresponding to the 1800-MHz band and becomes an in-phase  
25 baseband reception signal and a quadrature baseband reception

signal. The in-phase baseband reception signal passes through a low-pass filter 14 and is output to an in-phase baseband output terminal 16. The quadrature baseband reception signal passes through a low-pass filter 15 and is output to a quadrature baseband output terminal 17.

[0034]

When the multimode radio 100 operates in the 900-MHz mode, likewise a reception signal received at the antenna 1 is input to a low noise amplifier 11 corresponding to the 900-MHz band through the duplexer 3. The reception signal is amplified by the low noise amplifier 11. The amplified reception signal is quadrature-demodulated by a quadrature demodulator 13 corresponding to the 900-MHz band and becomes an in-phase baseband reception signal and a quadrature baseband reception signal. The in-phase baseband reception signal passes through the low-pass filter 14 and is output to the in-phase baseband output terminal 16. The quadrature baseband reception signal passes through the low-pass filter 15 and is output to the quadrature baseband output terminal 17. A frequency synthesizer has a local oscillator 18 for outputting a 3.6-GHz band signal and a frequency dividing section 22. The frequency synthesizer outputs an in-phase local oscillation signal and a quadrature local oscillation signal having a 90° phase difference to the quadrature modulators 6 and 7 and the quadrature demodulators 12 and 13.

[0035]

A frequency divider 19 divides output of the local oscillator 18 (3.6-GHz band) into two parts. A frequency divider 20 divides an in-phase local oscillation signal of the frequency divider 19 into two parts. A dummy circuit 21 is connected to the quadrature local oscillation signal side of the frequency divider 19. The frequency dividing section 22 is made up of the frequency divider 19, the frequency divider 20, and the dummy circuit 21. The frequency divider 19 outputs a 1800-MHz in-phase local oscillation signal and a 1800-MHz quadrature local oscillation signal to the quadrature modulator 6 or the quadrature demodulator 12. The frequency divider 20 outputs a 900-MHz in-phase local oscillation signal and a 900-MHz quadrature local oscillation signal to the quadrature modulator 7 or the quadrature demodulator 13. A control section 23 performs current control in accordance with the operation mode of the multimode radio 100. The control section 23 outputs a signal so as to turn off the current of circuits not in the operation mode and controls the circuit operation.

[0036]

FIG. 2 is a diagram to show an example of a current control method in the control section 23. FIG. 3 is a diagram to show the configuration of the frequency dividing section 22. The current control method will be discussed with FIG. 2 and then

the operation of the frequency dividing section 22 will be discussed with FIG. 3.

[0037]

In FIG. 2, a transistor 201, a transistor 202, a resistor 203, and a resistor 204 make up a current mirror circuit. At the current mirror circuit operation time, input current  $I_{in}$  flowing into the transistor 201 and the resistor 203 and output current  $I_{out}$  flowing into the transistor 202 and the resistor 204 have the following relationship: Letting the emitter area of the transistor 201 be  $N1$ , the emitter area of the transistor 202 be  $N2$ , the resistance value of the resistor 203 be  $R3$ , the resistance value of the resistor 204 be  $R4$ , and  $N1R3=N2R4$ , the output current  $I_{out}$  becomes  $I_{out}=(N2/N1) I_{in}$ . Therefore, the amplifier, the quadrature modulator, the quadrature demodulator, and the frequency divider are connected to a collector of the transistor 202.

[0038]

A transistor 205 and a current control terminal 206 make up a switch. When the current control terminal 206 is low, the transistor 205 is off. When the current control terminal 206 is high, the transistor 205 is on. Therefore, when the current control terminal 206 is low, the current  $I_{in}$  does not flow into the transistor 205 and flows into the transistor 201 and the current mirror circuit operates. When the current control 206 is high, the input current  $I_{in}$  does not flow into

the transistor 201 and flows through the transistor 205 and the current mirror circuit does not operate. Accordingly, the operation of the amplifier, the quadrature modulator, the quadrature demodulator, and the frequency divider of the multimode radio can be switched on/off. If the current control method is used, the control section 23 outputs a low signal to the circuit in the operation mode and a high signal to the circuit not in the operation mode for switching the circuit.

[0039]

Parts identical with those shown in FIG. 1 are denoted by the same reference numerals in FIG. 3. The frequency divider 19 has an input amplifier 301, a flip-flop circuit 302 at a master stage, a flip-flop circuit 303 at a slave stage, an in-phase output amplifier 304, and a quadrature output amplifier 305. Output of the local oscillator 18 is amplified by the input amplifier 301. The amplified output of the local oscillator 18 is input to clock inputs of the flip-flop circuit 302 and the flip-flop circuit 303. Q output of the flip-flop circuit 302 and D input of the flip-flop circuit 303 are connected. QB output of the flip-flop circuit 303 and D input of the flip-flop circuit 302 are connected.

[0040]

A 1800-MHz in-phase local oscillation signal provided by dividing an input signal of the local oscillator 18 into two parts is output from the Q output of the flip-flop circuit

302. The 1800-MHz in-phase local oscillation signal is amplified by the in-phase output amplifier 304. A 1800-MHz quadrature local oscillation signal provided by dividing the input signal of the local oscillator 18 into two parts and  
5 having the phase leading that of the 1800-MHz in-phase local oscillation signal by  $90^\circ$  is output from Q output of the flip-flop circuit 303. The 1800-MHz quadrature local oscillation signal is amplified by the quadrature output amplifier 305.

10 [0041]

The frequency divider 20 has an input amplifier 306 connected to the Q output of the flip-flop circuit 302, a flip-flop circuit 307 at a master stage, a flip-flop circuit 308 at a slave stage, an in-phase output amplifier 309, and  
15 a quadrature output amplifier 310. The 1800-MHz in-phase local oscillation signal of the flip-flop circuit 302 is amplified by the input amplifier 306. The amplified 1800-MHz in-phase local oscillation signal is input to clock inputs of the flip-flop circuit 307 and the flip-flop circuit 308. Q  
20 output of the flip-flop circuit 307 and D input of the flip-flop circuit 308 are connected. QB output of the flip-flop circuit 308 and D input of the flip-flop circuit 307 are connected. A 900-MHz in-phase local oscillation signal provided by dividing the 1800-MHz in-phase local oscillation signal of the  
25 frequency divider 19 into two parts is output from the Q output

of the flip-flop circuit 307. The 900-MHz in-phase local oscillation signal is amplified by the in-phase output amplifier 309. A 900-MHz quadrature local oscillation signal provided by dividing the 1800-MHz in-phase local oscillation signal of the frequency divider 19 into two parts and having the phase leading that of the 900-MHz in-phase local oscillation signal by 90° is output from Q output of the flip-flop circuit 308. The 900-MHz quadrature local oscillation signal is amplified by the quadrature output amplifier 310.

[0042]

This means that the 900-MHz in-phase local oscillation signal and the 900-MHz quadrature local oscillation signal output by the frequency divider 20 are provided by dividing the signal of the local oscillator 18 into four parts. A dummy circuit 21 is connected to the Q output of the flip-flop circuit 303. The frequency divider 20 and the control section 23 are connected. When the multimode radio 100 operates in the 1800-MHz mode, the frequency divider 20 is turned off.

[0043]

At the 1800-MHz mode operation time, the 1800-MHz in-phase local oscillation signal and the 1800-MHz quadrature local oscillation signal are output from the frequency divider 19. The turned-off frequency divider 20 is connected to the Q output of the flip-flop circuit 302 for outputting the

1800-MHz in-phase local oscillation signal. The dummy circuit 21 is connected to the Q output of the flip-flop circuit 303 for outputting the 1800-MHz quadrature local oscillation signal. Here, the dummy circuit 21 is made the same circuit  
5 as the input amplifier 306 of the turned-off frequency divider 20, whereby the turned-off frequency divider 20 and the dummy circuit 21 keep impedance symmetry. Thus, the highly accurate 90° phase difference between the 1800-MHz in-phase local oscillation signal and the 1800-MHz quadrature local  
10 oscillation signal can be provided. The dummy circuit 21 may have the circuit configuration of a part of the input amplifier 306. For example, if the input amplifier 306 has a transistor to which a signal is input, a load element, a current source circuit, a bias circuit, etc., a transistor having the same  
15 configuration as the transistor may be used as the dummy circuit 21. As the dummy circuit 21 is made closer to the same circuit configuration as the input amplifier 306, the phase difference with higher accuracy can be provided.

[0044]

20 At the transmission time, the control section 23 performs current control so that the power amplifier 4 and the quadrature modulator 6 are turned on and the low noise amplifier 10 and the quadrature demodulator 12 are turned off. At the reception  
time, the control section 23 performs current control so that  
25 the power amplifier 4 and the quadrature modulator 6 are turned



off and the low noise amplifier 10 and the quadrature demodulator 12 are turned on. At the transmission time, the turned-off quadrature demodulator 12 is connected to the frequency divider 19. However, the same circuit is connected  
5 to the 1800-MHz in-phase local oscillation signal and the 1800-MHz quadrature local oscillation signal and thus the input impedance symmetry is not affected. Likewise, at the reception time, the turned-off quadrature modulator 6 is connected to the frequency divider 19, but the same circuit  
10 is connected to the 1800-MHz in-phase local oscillation signal and the 1800-MHz quadrature local oscillation signal and thus the impedance symmetry is not affected.

[0045]

At this time, the use bands of the 1800-MHz band and the  
15 900-MHz band and the frequency bands of the local oscillator 18 are as listed in (Table 1). In (Table 1), Tx denotes the transmission time and Rx denotes the reception time. As seen from (Table 1), in the 1800-MHz band, the use band is a half the frequency band of the local oscillator 18; in the 900-MHz  
20 band, the use band becomes a quarter of the frequency band of the local oscillator 18.

[0046]

[Table 1]

Table 1

|   | 1800-MHz band |               | 900-MHz band  |               |
|---|---------------|---------------|---------------|---------------|
|   | Tx            | Rx            | Tx            | Rx            |
| Use band<br>[MHz]                                 | 1710-<br>1785 | 1805-<br>1880 | 880-<br>915   | 925-<br>960   |
| Frequency band of<br>local oscillator 18<br>[MHz] | 3420-<br>3570 | 3610-<br>3760 | 3520-<br>3660 | 3700-<br>3840 |

[0047]

Thus, the frequency dividers are shared among radio systems and are combined, so that a multimode radio whose circuit scale is lessened and simplified can be provided.

[0048]

In the description of the first embodiment, the circuit is assumed to be an unbalanced circuit, but may be a balanced circuit.

10 [0049]

The dummy circuit 21 may be made up of a resistor and a capacitor if the dummy circuit 21 has the same impedance as the input amplifier 306 of the turned-off frequency divider 20.

15 [0050]

In the first embodiment, the dummy circuit 21 is connected to the quadrature local oscillation signal side of the frequency divider 19 and the frequency divider 20 is

connected to the in-phase local oscillation signal, but the connection may be opposite.

[0051]

The dummy circuit 21 may be used not only to keep the  
5 90° phase difference, but also to keep the 180° phase difference.

[0052]

(Second embodiment)

In a second embodiment of the invention, the operation  
10 of a multimode radio for covering four frequency bands will be discussed.

[0053]

FIG. 4 shows a configuration example of a reception system of a multimode radio in the second embodiment. The  
15 multimode radio in the second embodiment is a multimode radio using four frequency bands. As a specific example, in the description to follow, it is assumed that the four bands are 1800-MHz band and 900-MHz band of GSM, 5.2-GHz band of IEEE 802.11a, and 2.4-GHz band of IEEE 802.11b. The operation modes  
20 are 1800-MHz mode, 900-MHz mode, 5.2-GHz mode, and 2.4-GHz mode. Parts identical with those shown in FIG. 1 are denoted by the same reference numerals in FIG. 4. An antenna 1 is shared among the 900-MHz band, the 1800-MHz band, the 2.4-GHz band, and the 5.2-GHz band. The antenna 1 is connected to a low noise  
25 amplifier 10, a low noise amplifier 11, a low noise amplifier

31 corresponding to the 2.4-GHz band, and a low noise amplifier  
32 corresponding to the 5.2-GHz band.

[0054]

When multimode radio 400 operates in the 1800-MHz mode,  
5 a reception signal received at the antenna 1 is amplified by  
the low noise amplifier 10. The amplified reception signal  
is quadrature-demodulated by a quadrature demodulator 12 and  
becomes an in-phase baseband reception signal and a quadrature  
baseband reception signal. The in-phase baseband reception  
10 signal passes through a low-pass filter 14 and is output to  
an in-phase baseband output terminal 16. The quadrature  
baseband reception signal passes through a low-pass filter 15  
and is output to a quadrature baseband output terminal 17.

[0055]

15 When the multimode radio 400 operates in the 900-MHz mode,  
likewise a reception signal received at the antenna 1 is  
amplified by the low noise amplifier 11. The amplified  
reception signal is quadrature-demodulated by a quadrature  
demodulator 13 and becomes an in-phase baseband reception  
20 signal and a quadrature baseband reception signal. The  
in-phase baseband reception signal passes through the low-pass  
filter 14 and is output to the in-phase baseband output terminal  
16. The quadrature baseband reception signal passes through  
the low-pass filter 15 and is output to the quadrature baseband  
25 output terminal 17.

[0056]

When the multimode radio 400 operates in the 2.4-GHz mode, a reception signal received at the antenna 1 is amplified by the low noise amplifier 31. The amplified reception signal is subjected to frequency conversion to an intermediate frequency of a 500-MHz band by a reception mixer 33 corresponding to the 2.4-GHz band. The reception signal which becomes the intermediate frequency is quadrature-demodulated by a quadrature demodulator 35 corresponding to the 500-MHz band and becomes an in-phase baseband reception signal and a quadrature baseband reception signal. The in-phase baseband reception signal passes through the low-pass filter 14 and is output to the in-phase baseband output terminal 16. The quadrature baseband reception signal passes through the low-pass filter 15 and is output to the quadrature baseband output terminal 17.

[0057]

When the multimode radio 400 operates in the 5.2-GHz mode, a reception signal received at the antenna 1 is amplified by the low noise amplifier 32. The amplified reception signal is subjected to frequency conversion to an intermediate frequency of a 1000-MHz band by a reception mixer 34 corresponding to the 5.2-GHz band. The reception signal which becomes the intermediate frequency is quadrature-demodulated by a quadrature demodulator 36 corresponding to the 1000-MHz

band and becomes an in-phase baseband reception signal and a quadrature baseband reception signal. The in-phase baseband reception signal passes through the low-pass filter 14 and is output to the in-phase baseband output terminal 16. The  
5 quadrature baseband reception signal passes through the low-pass filter 15 and is output to the quadrature baseband output terminal 17. A frequency synthesizer has a local oscillator 18 for outputting a 4.0-GHz band from 3.6 GHz and a frequency dividing section 40. The frequency synthesizer  
10 outputs an in-phase local oscillation signal and a quadrature local oscillation signal having a 90° phase difference to the quadrature demodulators 12, 13, 35, and 36. The frequency synthesizer outputs a local oscillation signal to the reception mixers 33 and 34.

15 [0058]

A frequency divider 19 divides output of the local oscillator 18 into two parts. A frequency divider 20 divides an in-phase local oscillation signal of the frequency divider 19 into two parts. A dummy circuit 37 is connected to the  
20 quadrature local oscillation signal side of the frequency divider 19. A frequency divider 38 divides an in-phase local oscillation signal of the frequency divider 20 into two parts. A dummy circuit 39 is connected to the quadrature local oscillation signal side of the frequency divider 20. The  
25 frequency dividing section 40 has the frequency divider 19,

the frequency divider 20, the dummy circuit 37, the frequency divider 38, and the dummy circuit 39. A control section 23 outputs a signal so as to turn off the circuits not in the operation mode and controls the circuit operation.

5 [0059]

FIG. 5 is a diagram to show the configuration of the frequency dividing section 40. Parts identical with those shown in FIG. 4 are denoted by the same reference numerals in FIG. 5. The frequency divider 19 has an input amplifier 301, a flip-flop circuit 302 at a master stage, a flip-flop circuit 303 at a slave stage, an in-phase output amplifier 304, and a quadrature output amplifier 305. Output of the local oscillator 18 is amplified by the input amplifier 301. The amplified output of the local oscillator 18 is input to clock inputs of the flip-flop circuit 302 and the flip-flop circuit 303. Q output of the flip-flop circuit 302 and D input of the flip-flop circuit 303 are connected. QB output of the flip-flop circuit 303 and D input of the flip-flop circuit 302 are connected. A 1800-MHz in-phase local oscillation signal provided by dividing an input signal (3.6-GHz band) of the local oscillator 18 into two parts is output from the Q output of the flip-flop circuit 302. The 1800-MHz in-phase local oscillation signal is amplified by the in-phase output amplifier 304. A 1800-MHz quadrature local oscillation signal provided by dividing the input signal of the local oscillator

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18 into two parts and having the phase leading that of the 1800-MHz in-phase local oscillation signal by 90° is output from Q output of the flip-flop circuit 303. The 1800-MHz quadrature local oscillation signal is amplified by the quadrature output amplifier 305. When the input signal of the local oscillator 18 is a 4.0-GHz band signal, a 2000-MHz in-phase local oscillation signal is output from the frequency divider 19 through an amplifier 506.

[0060]

The frequency divider 20 has an input amplifier 306 connected to the Q output of the flip-flop circuit 302, a flip-flop circuit 307 at a master stage, a flip-flop circuit 308 at a slave stage, an in-phase output amplifier 309, and a quadrature output amplifier 310. The 1800-MHz in-phase local oscillation signal is amplified by the input amplifier 306. The amplified 1800-MHz in-phase local oscillation signal is input to clock inputs of the flip-flop circuit 307 and the flip-flop circuit 308. Q output of the flip-flop circuit 307 and D input of the flip-flop circuit 308 are connected. QB output of the flip-flop circuit 308 and D input of the flip-flop circuit 307 are connected.

[0061]

A 900-MHz in-phase local oscillation signal provided by dividing the 1800-MHz in-phase local oscillation signal of the frequency divider 19 into two parts is output from the Q output



of the flip-flop circuit 307. The 900-MHz in-phase local oscillation signal is amplified by the in-phase output amplifier 309. A 900-MHz quadrature local oscillation signal provided by dividing the 1800-MHz in-phase local oscillation signal of the frequency divider 19 into two parts and having the phase leading that of the 900-MHz in-phase local oscillation signal by  $90^\circ$  is output from Q output of the flip-flop circuit 308. The 900-MHz quadrature local oscillation signal is amplified by the quadrature output amplifier 310. This means that the output of the frequency divider 20 is provided by dividing the signal of the local oscillator 18 (3.6-GHz band) into four parts. When the input signal of the local oscillator 18 is a 4.0-GHz band signal, a 1000-MHz in-phase local oscillation signal and a 1000-MHz quadrature local oscillation signal are output from the frequency divider 20.

[0062]

The frequency divider 38 has an input amplifier 501 connected to the Q output of the flip-flop circuit 307, a flip-flop circuit 502 at a master stage, a flip-flop circuit 503 at a slave stage, an in-phase output amplifier 504, and a quadrature output amplifier 505. The 1000-MHz in-phase local oscillation signal is amplified by the input amplifier 501. The amplified 1000-MHz in-phase local oscillation signal is input to clock inputs of the flip-flop circuit 502 and the

flip-flop circuit 503. Q output of the flip-flop circuit 502  
and D input of the flip-flop circuit 503 are connected. QB  
output of the flip-flop circuit 503 and D input of the flip-flop  
circuit 502 are connected. A 500-MHz in-phase local  
5 oscillation signal provided by dividing the 1000-MHz in-phase  
local oscillation signal of the frequency divider 20 into two  
parts is output from the Q output of the flip-flop circuit 502.  
The 500-MHz in-phase local oscillation signal is amplified by  
the in-phase output amplifier 504. A 500-MHz quadrature local  
10 oscillation signal provided by dividing the 1000-MHz in-phase  
local oscillation signal of the frequency divider 20 into two  
parts and having the phase leading that of the 500-MHz in-phase  
local oscillation signal by  $90^\circ$  is output from Q output of the  
flip-flop circuit 503. The 500-MHz quadrature local  
15 oscillation signal is amplified by the quadrature output  
amplifier 505. This means that the output of the frequency  
divider 38 is provided by dividing the input signal of the local  
oscillator 18 (4.0-GHz band) into eight parts.

[0063]

20 A dummy circuit 37 is connected to the Q output of the  
flip-flop circuit 303. A dummy circuit 39 is connected to the  
Q output of the flip-flop circuit 308.

[0064]

The control section 23 is connected to the frequency  
25 divider 20 and the frequency divider 38. The operation of the

frequency divider 20, 38 is switched on/off in response to the operation mode of the multimode radio 400. When the multimode radio 400 operates in the 1800-MHz mode, only the frequency divider 19 operates and outputs the 1800-MHz in-phase local oscillation signal and the 1800-MHz quadrature local oscillation signal to the quadrature demodulator 12. At this time, the frequency divider 20 and the frequency divider 38 are turned off by the control section 23. When the multimode radio 400 operates in the 900-MHz mode, the frequency divider 19 and the frequency divider 20 operate and output the 900-MHz in-phase local oscillation signal and the 900-MHz quadrature local oscillation signal to the quadrature demodulator 13. At this time, the frequency divider 38 is turned off by the control section 23.

15 [0065]

When the multimode radio 400 operates in the 2.4-GHz mode, the frequency divider 19, the frequency divider 20, and the frequency divider 38 operate. The frequency divider 19 outputs the 2000-MHz in-phase local oscillation signal to the reception mixer 33. The frequency divider 38 outputs the 500-MHz in-phase local oscillation signal and the 500-MHz quadrature local oscillation signal to the quadrature demodulator 35. When the multimode radio 400 operates in the 5.2-GHz mode, the frequency divider 19 and the frequency divider 20 operate. The local oscillator 18 outputs a

4000-MHz local oscillation signal to the reception mixer 34.  
The frequency divider 20 outputs the 1000-MHz in-phase local  
oscillation signal and the 1000-MHz quadrature local  
oscillation signal to the quadrature demodulator 36. At this  
5 time, the frequency divider 38 is turned off by the control  
section 23. The operation of the frequency dividing section  
40 for each operation mode of the multimode radio 400 is listed  
in (Table 2):

[0066]

10 [Table 2]

Table 2

|                               | Frequency<br>divider 19 | Frequency<br>divider 20 | Frequency<br>divider 38 |
|-------------------------------|-------------------------|-------------------------|-------------------------|
| At 900-MHz<br>operation time  | ON                      | ON                      | OFF                     |
| At 1800-MHz<br>operation time | ON                      | OFF                     | OFF                     |
| At 2.4-GHz<br>operation time  | ON                      | ON                      | ON                      |
| At 5.2-GHz<br>operation time  | ON                      | ON                      | OFF                     |

[0067]

At the 1800-MHz mode operation time, the turned-off  
5 frequency divider 20 and the turned-off amplifier 506 are  
connected to the Q output of the flip-flop circuit 302. However,  
the dummy circuit 37 is made the same circuit as the input  
amplifier 306 of the turned-off frequency divider 20 and the  
turned-off amplifier 506, whereby the impedance symmetry is  
10 kept. Thus, the highly accurate 90° phase difference between  
the 1800-MHz in-phase local oscillation signal and the 1800-MHz  
quadrature local oscillation signal can be provided. At the  
900-MHz mode operation time, the turned-off frequency divider  
38 is connected to the Q output of the flip-flop circuit 307.  
15 However, the dummy circuit 39 is made the same circuit as the

input amplifier 501 of the turned-off frequency divider 38,  
whereby the impedance symmetry is kept. Thus, the highly  
accurate 90° phase difference between the 900-MHz in-phase  
local oscillation signal and the 900-MHz quadrature local  
5 oscillation signal can be provided.

[0068]

The dummy circuit 37 may have the circuit configuration  
of a part of the input amplifier 306 and the amplifier 506,  
and the dummy circuit 39 may have the circuit configuration  
10 of a part of the input amplifier 501.

[0069]

Likewise, also at the 5.2-GHz operation time, the  
turned-off frequency divider 38 and the dummy circuit 39 keep  
the impedance balance. Thus, the 1000-MHz in-phase local  
15 oscillation signal and the 1000-MHz quadrature local  
oscillation signal can be provided. Output of the frequency  
divider 20 is connected to the quadrature demodulator 13 and  
the quadrature demodulator 36. At the 900-MHz operation time,  
the control section 23 performs current control so that the  
20 quadrature demodulator 13 is turned on and the quadrature  
demodulator 36 is turned off. At the 5.2-GHz operation time,  
the control section 23 performs current control so that the  
quadrature demodulator 13 is turned off and the quadrature  
demodulator 36 is turned on. At the 900-MHz operation time,  
25 the turned-off quadrature demodulator 36 is connected.

However, the same circuit is connected to the 900-MHz in-phase local oscillation signal and the 900-MHz quadrature local oscillation signal and thus the input impedance symmetry is not affected. Likewise, at the 5.2-GHz operation time, the  
5 turned-off quadrature demodulator 13 is connected, but the impedance symmetry is not affected.

[0070]

At this time, the use frequency bands of the local oscillator 18 for the use bands of the operation modes are as  
10 listed in (Table 3).

[0071]

[Table 3]

Table 3

|   | 900-MHz<br>band | 1800-MHz<br>band | 2.4-GHz<br>band | 5.2-GHz<br>band |
|---|-----------------|------------------|-----------------|-----------------|
| Use band<br>[MHz]                                 | 925-<br>960     | 1805-<br>1880    | 2400-<br>2483.5 | 5150-<br>5350   |
| Frequency band of<br>local oscillator 18<br>[MHz] | 3700-<br>3840   | 3610-<br>3760    | 3840-<br>3973.6 | 4120-<br>4280   |

15 [0072]

Thus, the frequency dividers are shared and are combined so as to cover a plurality of radio systems, so that a multimode radio whose circuit scale is lessened and simplified can be

provided.

[0073]

In the second embodiment, the reception system of the multimode radio has been described, but a transmission system  
5 can be realized in a similar manner, needless to say.

[0074]

In the second embodiment, the quadrature demodulators are provided in a one-to-one correspondence with the radio systems. However, using one quadrature demodulator  
10 corresponding to a plurality of radio systems, the local oscillation signal input to the quadrature demodulator may be switched for each radio system.

[0075]

In the second embodiment, GSM 1800-MHz band, GSM 900-MHz  
15 band, IEEE 802.11a, and IEEE 802.11b have been described as the radio systems. However, any other radio system may be adopted.

[0076]

The dummy circuit 37 may be made up of a resistor and  
20 a capacitor if the dummy circuit 37 has the same impedance as the input amplifier 306 of the turned-off frequency divider 20 and the amplifier 506.

[0077]

The dummy circuit 39 may be made up of a resistor and  
25 a capacitor if the dummy circuit 39 has the same impedance as



the input amplifier 501 of the turned-off frequency divider 38.

[0078]

In the second embodiment, the dummy circuit 37 is  
5 connected to the quadrature local oscillation signal side of  
the frequency divider 19 and the frequency divider 20 is  
connected to the in-phase local oscillation signal, but the  
connection may be opposite. The dummy circuit 39 is connected  
to the quadrature local oscillation signal side of the  
10 frequency divider 20 and the frequency divider 38 is connected  
to the in-phase local oscillation signal, but the connection  
may be opposite.

[0079]

The dummy circuits 37 and 39 may be used not only to keep  
15 the 90° phase difference, but also to keep the 180° phase  
difference.

[0080]

The number of the radio systems covered by the multimode  
radio is two in the first embodiment and four in the second  
20 embodiment. However, the number of the radio systems covered  
by the multimode radio is not limited to two or four and may  
be three or five or more.

[0081]

(Third embodiment)

25 FIG. 6 shows a configuration example of a multimode radio

in a third embodiment of the invention. A multimode radio 600 of the third embodiment uses a first frequency band and a second frequency band. As a specific example, in the description to follow, it is assumed that the radio system is GSM, the first  
5 frequency band is 1800-MHz band, and the second frequency band is 900-MHz band, but any other radio system and any other frequency band may be adopted. The operation modes are 1800-MHz mode and 900-MHz mode. Components identical with those described in the first embodiment of the invention are  
10 denoted by the same reference numerals in the third embodiment and will not be discussed again.

[0082]

In FIG. 6, a frequency divider 601 in a frequency dividing section 603 further divides a 1800-MHz in-phase local  
15 oscillation signal output by a frequency divider 19 into two parts. A dummy circuit 602 is connected to the quadrature local oscillation signal side of the frequency divider 19. At the 1800-MHz mode operation time, the frequency divider 19 outputs a 1800-MHz in-phase local oscillation signal and a 1800-MHz  
20 quadrature local oscillation signal to a quadrature demodulator 6 or a quadrature demodulator 12. At the 900-MHz mode operation time, the frequency divider 601 outputs a 900-MHz in-phase local oscillation signal and a 900-MHz quadrature local oscillation signal to a quadrature modulator  
25 7 or a quadrature modulator 13. A control section 23 is

connected to the frequency divider 601 and the dummy circuit 602 and outputs a signal in response to the operation mode of the multimode radio 600.

[0083]

5           FIG. 7 shows the configuration of the frequency dividing section 603. The dummy circuit 602 has the same circuit configuration as an input amplifier 604 of the frequency divider 601. At the 1800-MHz mode operation time, the control section 23 turns off a flip-flop 307, a flip-flop 308, an  
10 in-phase output amplifier 309, and a quadrature output amplifier 310 of the frequency divider 601. The input amplifier 604 and the dummy circuit 602 are turned on and allow current to flow. At this time, the control section 23 adjusts the current flowing into the input amplifier 604 and the dummy  
15 circuit 602. Thus, the phase difference between the 1800-MHz in-phase local oscillation signal and the 1800-MHz quadrature local oscillation signal can be adjusted.

[0084]

FIG. 8 is a circuit diagram to show an example of the  
20 input amplifier 604. From FIG. 8, the input amplifier 604 is a differential amplification circuit. Emitter terminals of a transistor 605 and a transistor 606 are connected to form a differential pair. The transistor 605 is connected to a voltage source via a load resistor 607. The transistor 606  
25 is connected to the voltage source via a load resistor 608.

The emitters of the transistors 605 and 606 are connected to a transistor 609 operating as a current source. A base of the transistor 609 is connected to the control section 23. The current flowing into the input amplifier 604 can be controlled  
5 by a signal voltage from the control section 23 fed into the base of the transistor 609. An emitter of the transistor 609 is grounded through a resistor 610. The dummy circuit 602 also has the same circuit configuration. The control section 23 can control the current flowing into the dummy circuit 602 by  
10 a signal. The dummy circuit 602 and the input amplifier 604 differ in that the dummy circuit 602 does not output an amplified signal.

[0085]

When the multimode radio 600 operates in the 900-MHz mode,  
15 the 1800-MHz in-phase local oscillation signal output from the frequency divider 19 is input to the transistor 605 and the transistor 606. The 1800-MHz in-phase local oscillation signal is subjected to voltage conversion through the load resistor 607 and the load resistor 608 and is output from a  
20 collector of the transistor 605 and a collector of the transistor 606 to a flip-flop 307 and a flip-flop 308.

[0086]

When the multimode radio 600 operates in the 1800-MHz mode, the input amplifier 604 and the dummy circuit 602 are  
25 subjected to current control by a signal from the control

section 23. Thus, the input impedances of the input amplifier 604 and the dummy circuit 602 viewed from the frequency divider 19 change. The control section 23 outputs the signal to the input amplifier 604 and the dummy circuit 602 so that the phase  
5 difference between the 1800-MHz in-phase local oscillation signal and the 1800-MHz quadrature local oscillation signal output from the frequency divider 19 becomes 90°. At this time, the current flowing into the input amplifier 604 may be made smaller than the current flowing at the 900-MHz mode operation  
10 time for controlling the phase difference, and the power consumption of the multimode radio 600 can be suppressed.  
[0087]

Thus, the frequency dividers are shared among radio systems and are combined, so that a multimode radio whose  
15 circuit scale is lessened and simplified can be provided.  
[0088]

In the third embodiment, the input amplifier 604 and the dummy circuit 602 are each a balanced differential amplification circuit, but may be each an unbalanced circuit.  
20 [0089]

In the third embodiment, the dummy circuit 602 is connected to the quadrature local oscillation signal side of the frequency divider 19 and the frequency divider 601 is connected to the in-phase local oscillation signal side, but  
25 the connection may be opposite.

[0090]

In the third embodiment, the current flowing into the input amplifier 604 and the dummy circuit 602 is controlled by the signal from the control section 23. However, the current  
5 flowing into the dummy circuit 602 may be controlled by the signal from the control section 23 as the current flowing into the input amplifier 604 is fixed. The current flowing into the input amplifier 604 may be controlled by the signal from the control section 23 as the current flowing into the dummy  
10 circuit 602 is fixed. In this case, the circuit configuration of the dummy circuit 602 may be the same as the circuit configuration of a part of the input amplifier 604 of the frequency divider 601.

[0091]

15 (Fourth embodiment)

FIG. 9 shows a configuration example of a multimode radio in a fourth embodiment of the invention. A multimode radio 700 of the fourth embodiment uses a first frequency band and a second frequency band. As a specific example, in the  
20 description to follow, it is assumed that the radio system is GSM, the first frequency band is 1800-MHz band, and the second frequency band is 900-MHz band. The operation modes are 1800-MHz mode and 900-MHz mode. Components identical with those described in the first embodiment of the invention are  
25 denoted by the same reference numerals in the fourth embodiment

and will not be discussed again.

[0092]

In FIG. 9, a frequency divider 701 in a frequency dividing section 702 is a circuit for dividing output of a local oscillator 18 (3.6-GHz band) into two parts. A frequency divider 20 is a circuit for further dividing a 1800-MHz in-phase local oscillation signal output by the frequency divider 701 into two parts. At the 1800-MHz mode operation time, the frequency divider 701 outputs a 1800-MHz in-phase local oscillation signal and a 1800-MHz quadrature local oscillation signal to a quadrature demodulator 6 or a quadrature demodulator 12. At the 900-MHz mode operation time, the frequency divider 20 outputs a 900-MHz in-phase local oscillation signal and a 900-MHz quadrature local oscillation signal to a quadrature modulator 7 or a quadrature modulator 13. A control section 23 is connected to the frequency divider 20 and the frequency divider 701 and outputs a signal in response to the operation mode of the multimode radio 700.

[0093]

FIG. 10 shows the configuration of the frequency dividing section 702. At the 1800-MHz mode operation time, the control section 23 turns off an input amplifier 306, a flip-flop 307, a flip-flop 308, an in-phase output amplifier 309, and a quadrature output amplifier 310 of the frequency divider 20. At this time, the control section 23 can adjust the phase

difference between the 1800-MHz in-phase local oscillation signal and the 1800-MHz quadrature local oscillation signal by adjusting the current flowing into an in-phase output amplifier 703 and a quadrature output amplifier 704.

5 [0094]

FIG. 11 is a circuit diagram to show an example of the in-phase output amplifier 703. From FIG. 11, the in-phase output amplifier 703 is a differential amplification circuit. Emitter terminals of a transistor 705 and a transistor 706 are connected to form a differential pair. The transistor 705 is connected to a voltage source via a load resistor 707. The transistor 706 is connected to the voltage source via a load resistor 708. The emitters of the transistors 705 and 706 are connected to a transistor 709 operating as a current source. A base of the transistor 709 is connected to the control section 23. The current flowing into the in-phase output amplifier 703 can be controlled by a signal voltage from the control section 23 fed into the base of a transistor 709. An emitter of the transistor 709 is grounded through a resistor 710. The quadrature output amplifier 704 also has the same circuit configuration and the current flowing into the quadrature output amplifier 704 can be controlled by a signal from the control section 23.

[0095]

25 When the multimode radio 700 operates in the 1800-MHz



mode, the in-phase output amplifier 703 and the quadrature output amplifier 704 are subjected to current control by a signal from the control section 23. Thus, the input impedances of the in-phase output amplifier 703 and the quadrature output amplifier 704 change. The control section 23 outputs the signal to the in-phase output amplifier 703 and the quadrature output amplifier 704 so that the phase difference between the 1800-MHz in-phase local oscillation signal and the 1800-MHz quadrature local oscillation signal output from the frequency divider 701 becomes 90°.

[0096]

Thus, the frequency dividers are shared among radio systems and are combined, so that a multimode radio whose circuit scale is lessened and simplified can be provided.

[0097]

In the fourth embodiment, the in-phase output amplifier 703 and the quadrature output amplifier 704 are each a balanced differential amplification circuit, but may be each an unbalanced circuit.

[0098]

In the fourth embodiment, the frequency divider 20 is connected to the in-phase local oscillation signal side, but may be connected to the quadrature local oscillation signal side.

[0099]

In the fourth embodiment, the current flowing into the in-phase output amplifier 703 and the quadrature output amplifier 704 is controlled by the signal from the control section 23. However, the current flowing into the quadrature output amplifier 704 may be controlled by the signal from the control section 23 as the current flowing into the in-phase output amplifier 703 is fixed. The current flowing into the in-phase output amplifier 703 may be controlled by the signal from the control section 23 as the current flowing into the quadrature output amplifier 704 is fixed.

[0100]

(Fifth embodiment)

FIG. 12 shows a configuration example of a multimode radio in a fifth embodiment of the invention. A multimode radio 800 of the fifth embodiment uses a first frequency band and a second frequency band. As a specific example, in the description to follow, it is assumed that the radio system is GSM, the first frequency band is 1800-MHz band, and the second frequency band is 900-MHz band, but any other radio system and any other frequency band may be adopted. The operation modes are 1800-MHz mode and 900-MHz mode. Components identical with those described in the first to fourth embodiments of the invention are denoted by the same reference numerals in the fifth embodiment and will not be discussed again.

[0101]

In FIG. 12, a frequency divider 601 in a frequency dividing section 801 is a circuit for further dividing a 1800-MHz in-phase local oscillation signal output by a frequency divider 701 into two parts. A dummy circuit 602 is  
5 connected to the quadrature local oscillation signal side of the frequency divider 701. At the 1800-MHz mode operation time, the frequency divider 701 outputs a 1800-MHz in-phase local oscillation signal and a 1800-MHz quadrature local oscillation signal to a quadrature demodulator 6 or a quadrature  
10 demodulator 12. At the 900-MHz mode operation time, the frequency divider 601 outputs a 900-MHz in-phase local oscillation signal and a 900-MHz quadrature local oscillation signal to a quadrature modulator 7 or a quadrature modulator 13. A control section 23 is connected to the frequency divider  
15 701, the frequency divider 601, and the dummy circuit 602 and outputs a signal in response to the operation mode of the multimode radio 800.

[0102]

FIG. 13 shows the configuration of the frequency dividing  
20 section 801. The dummy circuit 602 has the same circuit configuration as an input amplifier 604 of the frequency divider 601. At the 1800-MHz mode operation time, the control section 23 turns off a flip-flop 307, a flip-flop 308, an in-phase output amplifier 309, and a quadrature output  
25 amplifier 310 of the frequency divider 601. The input

amplifier 604 is turned on and allows current to flow. The dummy circuit 602 is also turned on by a signal from the control section 23 and allows current to flow. At this time, the control section 23 controls the current flowing into the input amplifier 604, the dummy circuit 602, the in-phase output amplifier 703, and the quadrature output amplifier 704. Thus, the phase difference between the 1800-MHz in-phase local oscillation signal and the 1800-MHz quadrature local oscillation signal can be adjusted.

10 [0103]

Thus, the frequency dividers are shared among radio systems and are combined, so that a multimode radio whose circuit scale is lessened and simplified can be provided.

[0104]

15 In the description of the fifth embodiment, it is assumed that the circuit is an unbalanced circuit, but the circuit may be a balanced circuit.

[0105]

20 In the fifth embodiment, the dummy circuit 602 is connected to the quadrature local oscillation signal side of the frequency divider 701 and the frequency divider 601 is connected to the in-phase local oscillation signal side, but the connection may be opposite.

[0106]

25 In the fifth embodiment, the current flowing into the

input amplifier 604, the dummy circuit 602, the in-phase output amplifier 703, and the quadrature output amplifier 704 is controlled by the signal from the control section 23. However, the current flowing into any one of the components may be controlled. The current flowing into any two of the components may be controlled. The current flowing into any three of the components may be controlled. To control the current flowing into only either the dummy circuit 602 or the input amplifier 604, the circuit configuration of the dummy circuit 602 may be the same as the circuit configuration of a part of the input amplifier 604 of the frequency divider 601.

[0107]

While the invention has been described in detail with reference to the specific embodiments, it will be obvious to those skilled in the art that various changes and modifications can be made without departing from the spirit and the scope of the invention.

[0108]

The present application is based on Japanese Patent Application (No. 2004-60388) filed on March 4, 2004 and Japanese Patent Application (No. 2005-47649) filed on February 23, 2005, which are incorporated herein by reference.

INDUSTRIAL APPLICABILITY

[0109]

The multimode radio according to the invention has the advantage that the circuit scale is lessened and simplified by sharing and combining frequency dividers compatible with different radio systems, is useful in the communication field, etc., and can be used with electric machines relating to communications, for example, a mobile telephone, a wireless LAN, etc.